

# D0 Upgrade Electronics

## Parsing the Tracking into Multiple FPLDs

### Version 1

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#### 1. Introduction

"How many and what size FPLD's are needed for the CFT Trigger FE boards?" This note answers that question for three different design options. These design options are:

- 1 - 6 of the largest FPLD's
- 2 - 16 smaller FPLD's in a 2x8 array (2=>Pt sign, 8=>Pt range)
- 3 - 16 smaller FPLD's in a 2x2x4 array (2=>Pt sign, 2=>1/2 phi bin, 4=>Pt range)

The major reason we chose FPLD's for the L1 trigger is generality. That is the details of the trigger could be concentrated in the programming of a hardware device while the hardware layout of the PCB could be made as general as possible. The programming then could be modified at any time in the development cycle and even during the running cycle without any modifications to the underlying PCB. To this end our preferred hardware design delivers all the fiber (and preshower) channels to each of several FPLD's on the FE PCB. The first option listed above is built on this premiss. It might, however, be advisable for cost and complexity reasons to tailor the FE PBC for more FPLD's that have only some of the total available input channels. This tailored board might still be general enough to meet our initial goals while offering a more cost effective board. The 2<sup>nd</sup> and 3<sup>rd</sup> options above explore this possibility.

#### 2. Technique

To conduct this study I created a series of worksheets. Please see table 1 which has three copies of the basic worksheet. On each sheet the minimum and maximum Pt ranges and the minimum and maximum fiber bins are entered. The sheet then calculates the number of input pins are needed. It also calculates the offset value for each Pt value and from the offset values and the

fiber bin ranges calculates the approximate number of equations needed. The formula for the number of equations is number-of-fiber-bins-at-H-layer x number-of-offset-bins x 12. There is of course a set of equations for each outer layer bin and offset. The total number of bins is then some factor times the product of these two values. Inspection of the generated table of equations indicates that this factor is about 12. Inspection of the entries of the table shows that each of the six intervening layers has on average two different values in the table. Two for each times six layers is twelve.

Table 1 has the number of pins and equations for the total Pt range of –1.5 to +1.5 GeV. These numbers check with those found other ways. The second and third sheets further check the spread sheet calculations.

Table 2 shows for comparison the total numbers of pins and equations for four different values for the global minimum Pt. Table 3 is the same but with only one sign of the Pt. The number of equations are as expected  $\frac{1}{2}$  the number and the number of pins varies as expected. In table 4 the total Pt range for one sign is split into four non-overlapping Pt ranges. Table 5 and 6 are for the same Pt ranges but with the H layer range  $\frac{1}{2}$  and  $\frac{1}{4}$  of a sector respectively. We see that the number of equations decreases exactly as the range factors but the number of pins, especially for the lowest Pt range does not increase as quickly.

Starting with table 7 extra calculations are added to each spread sheet. From the total number of equations the number of Logic Elements, LE, needed for the equations by multiplying the number of equations by 3.0. Experience has shown that the actual factor is at least 2.5 but less than 3.0. The other major user of LE's in the FPLD's is the code which converts the found tracks to the Pt/phi code for output. The sheet uses the known size for a given Pt by phi size and scales it to the size in the sheet. Priority coding for serialization, done on 11/10/97 in file n\_main\_1 uses 1743 LC's for a 48 x 6 pin array. For a full 48 x 24 one would need 6972 LC's. The total number of LE's is then found and compared to different available FPLD models. The comparison of pins to that available for different FPLD models is made in the text.

### 3. The Options

#### 3.1 Six Large FPLD's

This design parses the tracking problem into six of the largest FPLD's that will be available at the start of the run. The parsing is:

Chip	Use
1	Highest Pt Threshold bin
2	High Pt Threshold bin
3	Medium Pt Threshold bin, Positive track curvature
4	Medium Pt Threshold bin, Negative track curvature
5	Low Pt Threshold bin, Positive track curvature
6	Low Pt Threshold bin, Negative track curvature

Tables 7 and 8 show the estimated resources needed for this design. Most of the chips are at a utilization level of 72% of a 10K250. The exception is the high Pt threshold bin, which uses 85% of the chip. The total number of pins is fairly constant for each chip. The 10K250 will have 470 I/O pins in a pin grid package of 599 pins or a ball grid array package of 600 pins. Therefore the I/O will have to be multiplexed with at least a factor of 2. The planned factor of 4 ensures a large number of free pins.

The 10K250 chip is not included on the cost sheet for Q1 1998. But if we use the cost of the largest chip there, with the fastest speed, and for quantities of over 500, the cost is \$1860 each.

Description	Number	Cost
Each Chip	1	\$ 1,860
Each FE Board	6	\$ 11,160
Entire CFT	528	\$ 982,080

This leads to a very large total cost. But we can expect the cost of this chip to drop over the next year. If we use the present cost for this chip in the slowest speed grade as the estimated cost of the largest and fastest then we get:

Description	Number	Cost
Each Chip	1	\$ 840
Each FE Board	6	\$ 5,040
Entire CFT	528	\$ 443,520

which is still much larger than our planned cost.

The 600 lead BGA is a square 1.8" on a side and the 599 lead PGA is a square 2.46" on a side. Six of the PGA chips would fit tightly in a single row from front to back of the board. Six of the BGA chips would fit very nicely.

### 3.2 Sixteen FPLD's in a 2x8 Array

This design parses the tracking problem into sixteen smaller FPLD's that are available now. The parsing is:

Chip	Use
1	Highest Pt Range, Positive track curvature
2	Highest Pt Range, Negative track curvature
3	Next highest Pt Range, Positive track curvature
4	Next highest Pt Range, Negative track curvature
5	Next highest Pt Range, Positive track curvature
6	Next highest Pt Range, Negative track curvature
7	Next highest Pt Range, Positive track curvature
8	Next highest Pt Range, Negative track curvature
9	Next highest Pt Range, Positive track curvature
10	Next highest Pt Range, Negative track curvature
11	Next highest Pt Range, Positive track curvature
12	Next highest Pt Range, Negative track curvature
13	Next highest Pt Range, Positive track curvature

- 14 Next highest Pt Range, Negative track curvature
- 15 Lowest Pt Range, Positive track curvature
- 16 Lowest Pt Range, Negative track curvature

Tables 9 and 10 show the estimated resources needed for this design. All of the chips are at a utilization level of 80% of a 10K100 (61% of a 10K130). The total number of pins is fairly constant for each chip. The 10K100 has 274 I/O pins in a ball grid array package of 356 pins. Therefore the I/O will have to be multiplexed with at least a factor of 2. The planned factor of 4 ensures a large number of free pins. It is also available in a 240 lead quad flat pack with 189 I/O channels. With a x4 multiplexing this package could also be used. We have the technology and experience for using a QFP and none for the BGA..

Putting equal numbers of equations in each PLD has a bad side effect. The range Offset values of each chip no longer line up very well with even and integer offsets. The first four chips cover the range from +2.8 to -2.8, where a single large chip covered +2 to -2 for the highest Pt threshold in the first design.

The EPF10K100ABC356-1 chip is \$372 on the cost sheet for Q1 1998. This is the A version of the chip which is faster and a smaller process.

Description	Number	Cost
Each Chip	1	\$ 372
Each FE Board	16	\$ 5,952
Entire CFT	1408	\$ 523,776

We can expect the price for the chips to drop over 40% per annum. That reduces the price to \$314K first quarter of '99 and \$190K first quarter '20. Also we might instead of taking a price break use 10K130's. This chip is just out so the present price is not a good guide for future price. But we can expect its price to follow about 1 year behind the 10K100. Thus it could be purchased for \$314K in first quarter '20.

The 356 BGA has a square footprint 1.38" on a side. Allowing a between chip spacing of only 10% of the length gives 1.5" on a side. Eight chips in a row would need 12" by 3" for a total area of 36 sq in. The 240 lead QFP is almost the same size and would require the same space.

### 3.3 Sixteen FPLD's in a 2x2x4 Array

This design also parses the tracking problem into sixteen smaller FPLD's that are available now. But unlike the previous 2x8 design the trigger sector is divided into two halves in phi and only 4 Pt groups. The parsing is:

- | Chip | Use  |
|------|--|
| 1    | Highest Pt Range, Positive track curvature, Left half of phi       |
| 2    | Highest Pt Range, Positive track curvature, Right half of phi      |
| 3    | Highest Pt Range, Negative track curvature, Left half of phi       |
| 4    | Highest Pt Range, Negative track curvature, Right half of phi      |
| 5    | Next highest Pt Range, Positive track curvature, Left half of phi  |
| 6    | Next highest Pt Range, Positive track curvature, Right half of phi |
| 7    | Next highest Pt Range, Negative track curvature, Left half of phi  |

- 8 Next highest Pt Range, Negative track curvature, Right half of phi
- 9 Next highest Pt Range, Positive track curvature, Left half of phi
- 10 Next highest Pt Range, Positive track curvature, Right half of phi
- 11 Next highest Pt Range, Negative track curvature, Left half of phi
- 12 Next highest Pt Range, Negative track curvature, Right half of phi
- 13 Lowest Pt Range, Positive track curvature, Left half of phi
- 14 Lowest Pt Range, Positive track curvature, Right half of phi
- 15 Lowest Pt Range, Negative track curvature, Left half of phi
- 16 Lowest Pt Range, Negative track curvature, Right half of phi

Table 11 shows the estimated resources needed for this design. All of the chips are at a utilization level of 80% of a 10K100 (61% of a 10K130). Exactly as for the above design. The total number of pins is fairly constant for each chip, but now the number of pins is about  $\frac{1}{2}$  the above design. But the I/O will still have to be multiplexed with at least a factor of 2 in the 240 lead QFP or the 356 lead BGA. The planned factor of 4 ensures a large number of free pins.

The pricing for the chips is the same as the previous design.

### **3.4 More and Smaller FPLD's**

We could follow the sector splitting further and divide each sector into quarters and use 32 10K50 chips, which are about  $\frac{1}{2}$  the capacity in the same lead package. The price reduction though is only about 2/3 so if you multiply this by double the number of chips the price change ratio becomes 4/3. Thus putting 32 of the smallest chips raises the cost by 1/3. It would also of course greatly increase the board space needed. The 240 lead QFP has a square footprint 1.38" on a side, as stated above. Eight chips in a row would need 12" by 6" and 32 chips for a total area of 72 sq in.

## **4. Summary**

There are two different methods of parsing the problem into FPLD's which are viable, options 1 and 3. Option 1 is our base-line design. It uses the fewest FPLD's, 6, and has a full set of fiber inputs to each FPLD. Option 3 uses 16 FPLD's and splits the problem at the PCB level into sign-of-Pt and  $\frac{1}{2}$  sectors. The principle gain from this design is it allows us to back off from using the largest FPLD available and therefore avoid any associated cost penalty.

Design	#	Cost each	1998	1999	2000	2001
option 1	6	\$ 1,860	\$ 982	\$ 444	\$ 266	
Option 3 w 10K100	16	\$ 372	\$ 524	\$ 314	\$ 189	\$ 113
Option 3 w 10K130	16			\$ 524	\$ 314	\$ 189

This table summarizes the earlier cost tables and shows that the 16 chip options are less expensive under our assumptions for the price reduction of the chips in the future. For the 10K100 I took the present quoted price and multiplied by 0.6 for each succeeding year. For the 10K130 chip I took the '98 10K100 price as the '99 base price and reduced it by 0.6 per year. For the 10K250 in '99 price I

took the present 10K130 price for the fastest speed grade, and multiplied that price by 0.45 for the '00 price and by 0.6 for the '01 price.

What has not been discussed is the extra logic needed to combine the results of 16 FPLD's versus that from 6.

We shall continue to study both options for possible inclusion on the first prototype board.

Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1.5	45	88	-1.5	45	88		45	88	44
500	1.5	35.9	75.0	-1.5	45.9	85.0		35	85	51
450	1.5	27.8	63.0	-1.5	45.8	81.0		27	81	55
400	1.5	20.7	52.0	-1.5	44.7	76.0		20	76	57
350	1.5	14.6	42.0	-1.5	42.6	70.0		14	70	57
300	1.5	9.5	33.0	-1.5	39.5	63.0		9	63	55
250	1.5	5.5	25.0	-1.5	35.5	55.0		5	55	51
200	1.5	2.4	18.0	-1.5	30.4	46.0		2	46	45
	Offset	-14.0		Offset	14.0					
		Approx. Number of Equations		14616			Total Number of Pins	830		
		0.0003								
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1000	45	88	1000	45	88		45	88	44
500	1000	40.9	80.0	1000	40.9	80.0		40	80	41
450	1000	36.8	72.0	1000	36.8	72.0		36	72	37
400	1000	32.7	64.0	1000	32.7	64.0		32	64	33
350	1000	28.6	56.0	1000	28.6	56.0		28	56	29
300	1000	24.5	48.0	1000	24.5	48.0		24	48	25
250	1000	20.4	40.0	1000	20.4	40.0		20	40	21
200	1000	16.3	32.0	1000	16.3	32.0		16	32	17
	Offset	0.0		Offset	0.0					
		Approx. Number of Equations		504			Total Number of Pins	494		
		0.0003								
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1000	45	45	1000	45	45		45	45	1
500	1000	40.9	80.0	1000	40.9	80.0		40	80	41
450	1000	36.8	72.0	1000	36.8	72.0		36	72	37
400	1000	32.7	64.0	1000	32.7	64.0		32	64	33
350	1000	28.6	56.0	1000	28.6	56.0		28	56	29
300	1000	24.5	48.0	1000	24.5	48.0		24	48	25
250	1000	20.4	40.0	1000	20.4	40.0		20	40	21
200	1000	16.3	32.0	1000	16.3	32.0		16	32	17
	Offset	15.6		Offset	15.6					
		Approx. Number of Equations		12			Total Number of Pins	408		

**Table 1 Test of the spread sheet calculations.**

Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1.5	45	88	-1.5	45	88		45	88	44
500	1.5	35.9	75.0	-1.5	45.9	85.0		35	85	51
450	1.5	27.8	63.0	-1.5	45.8	81.0		27	81	55
400	1.5	20.7	52.0	-1.5	44.7	76.0		20	76	57
350	1.5	14.6	42.0	-1.5	42.6	70.0		14	70	57
300	1.5	9.5	33.0	-1.5	39.5	63.0		9	63	55
250	1.5	5.5	25.0	-1.5	35.5	55.0		5	55	51
200	1.5	2.4	18.0	-1.5	30.4	46.0		2	46	45
Offset		-14.0	Offset	14.0						
		Approx. Number of Equations			14616			Total Number of Pins		830
		0.0003								
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	2.63	45	88	-2.63	45	88		45	88	44
500	2.63	38.1	77.1	-2.63	43.8	82.9		38	83	46
450	2.63	31.7	66.9	-2.63	42.0	77.1		31	77	47
400	2.63	25.9	57.2	-2.63	39.6	70.8		25	71	47
350	2.63	20.7	48.0	-2.63	36.6	64.0		20	64	45
300	2.63	16.0	39.4	-2.63	33.1	56.6		15	57	43
250	2.63	11.9	31.4	-2.63	29.0	48.6		11	49	39
200	2.63	8.4	24.0	-2.63	24.3	40.0		8	40	33
Offset		-8.0	Offset	8.0						
		Approx. Number of Equations			8553			Total Number of Pins		688
		0.0003								
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	5.2	45	88	-5.2	45	88		45	88	44
500	5.2	39.5	78.6	-5.2	42.4	81.4		39	81	43
450	5.2	34.2	69.4	-5.2	39.4	74.6		34	75	42
400	5.2	29.3	60.5	-5.2	36.2	67.5		29	67	39
350	5.2	24.6	52.0	-5.2	32.7	60.0		24	60	37
300	5.2	20.2	43.7	-5.2	28.9	52.3		20	52	33
250	5.2	16.1	35.7	-5.2	24.8	44.3		16	44	29
200	5.2	12.3	28.0	-5.2	20.4	36.0		12	36	25
Offset		-4.0	Offset	4.0						
		Approx. Number of Equations			4575			Total Number of Pins		584
		0.0003								
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	10.5	45	88	-10.5	45	88		45	88	44
500	10.5	40.2	79.3	-10.5	41.6	80.7		40	81	42
450	10.5	35.5	70.7	-10.5	38.1	73.3		35	73	39
400	10.5	31.0	62.3	-10.5	34.4	65.7		31	66	36
350	10.5	26.6	54.0	-10.5	30.6	58.0		26	58	33
300	10.5	22.4	45.9	-10.5	26.7	50.1		22	50	29
250	10.5	18.3	37.9	-10.5	22.6	42.1		18	42	25
200	10.5	14.4	30.0	-10.5	18.4	34.0		14	34	21
Offset		-2.0	Offset	2.0						
		Approx. Number of Equations			2520			Total Number of Pins		538

**Table 2 Total number of equations needed for different Minimum Pt values.**

Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1000	45	88	1.5	45	88		45	88	44
500	1000	40.9	80.0	1.5	35.9	75.0		35	80	46
450	1000	36.8	72.0	1.5	27.8	63.0		27	72	46
400	1000	32.7	64.0	1.5	20.7	52.0		20	64	45
350	1000	28.6	56.0	1.5	14.6	42.0		14	56	43
300	1000	24.5	48.0	1.5	9.5	33.0		9	48	40
250	1000	20.4	40.0	1.5	5.5	25.0		5	40	36
200	1000	16.3	32.0	1.5	2.4	18.0		2	32	31
		Approx. Number of Equations				7067			Total Number of Pins	662
		0.0003								
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1000	45	88	3	45	88		45	88	44
500	1000	40.9	80.0	3	38.4	77.5		38	80	43
450	1000	36.8	72.0	3	32.3	67.5		32	72	41
400	1000	32.7	64.0	3	26.7	58.0		26	64	39
350	1000	28.6	56.0	3	21.6	49.0		21	56	36
300	1000	24.5	48.0	3	17.0	40.5		17	48	32
250	1000	20.4	40.0	3	13.0	32.5		12	40	29
200	1000	16.3	32.0	3	9.4	25.0		9	32	24
		Approx. Number of Equations				3539			Total Number of Pins	576
		0.0003								
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1000	45	88	5	45	88		45	88	44
500	1000	40.9	80.0	5	39.4	78.5		39	80	42
450	1000	36.8	72.0	5	34.1	69.3		34	72	39
400	1000	32.7	64.0	5	29.1	60.4		29	64	36
350	1000	28.6	56.0	5	24.4	51.8		24	56	33
300	1000	24.5	48.0	5	20.0	43.5		20	48	29
250	1000	20.4	40.0	5	16.0	35.5		15	40	26
200	1000	16.3	32.0	5	12.2	27.8		12	32	21
		Approx. Number of Equations				2127			Total Number of Pins	540
		0.0003								
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1000	45	88	8	45	88		45	88	44
500	1000	40.9	80.0	8	40.0	79.1		39	80	42
450	1000	36.8	72.0	8	35.1	70.3		35	72	38
400	1000	32.7	64.0	8	30.5	61.8		30	64	35
350	1000	28.6	56.0	8	26.0	53.4		26	56	31
300	1000	24.5	48.0	8	21.7	45.2		21	48	28
250	1000	20.4	40.0	8	17.6	37.2		17	40	24
200	1000	16.3	32.0	8	13.7	29.4		13	32	20
		Approx. Number of Equations				1334			Total Number of Pins	524

**Table 3 Total number of equations needed for different Minimum Pt values for tracks with a single curvature.**

Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1000	45	88	10.5	45	88		45	88	44
500	1000	40.9	80.0	10.5	40.2	79.3		40	80	41
450	1000	36.8	72.0	10.5	35.5	70.7		35	72	38
400	1000	32.7	64.0	10.5	31.0	62.3		31	64	34
350	1000	28.6	56.0	10.5	26.6	54.0		26	56	31
300	1000	24.5	48.0	10.5	22.4	45.9		22	48	27
250	1000	20.4	40.0	10.5	18.3	37.9		18	40	23
200	1000	16.3	32.0	10.5	14.4	30.0		14	32	19
	Offset	0.0		Offset	-2.0					
		Approx. Number of Equations		1501			Total Number of Pins		514	
		0.0003								
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	10.5	45	88	5.2	45	88		45	88	44
500	10.5	40.2	79.3	5.2	39.5	78.6		39	79	41
450	10.5	35.5	70.7	5.2	34.2	69.4		34	71	38
400	10.5	31.0	62.3	5.2	29.3	60.5		29	62	34
350	10.5	26.6	54.0	5.2	24.6	52.0		24	54	31
300	10.5	22.4	45.9	5.2	20.2	43.7		20	46	27
250	10.5	18.3	37.9	5.2	16.1	35.7		16	38	23
200	10.5	14.4	30.0	5.2	12.3	28.0		12	30	19
	Offset	-2.0		Offset	-4.0					
		Approx. Number of Equations		1531			Total Number of Pins		514	
		0.0003								
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	5.2	45	88	2.63	45	88		45	88	44
500	5.2	39.5	78.6	2.63	38.1	77.1		38	79	42
450	5.2	34.2	69.4	2.63	31.7	66.9		31	69	39
400	5.2	29.3	60.5	2.63	25.9	57.2		25	61	37
350	5.2	24.6	52.0	2.63	20.7	48.0		20	52	33
300	5.2	20.2	43.7	2.63	16.0	39.4		15	44	30
250	5.2	16.1	35.7	2.63	11.9	31.4		11	36	26
200	5.2	12.3	28.0	2.63	8.4	24.0		8	28	21
	Offset	-4.0		Offset	-8.0					
		Approx. Number of Equations		2493			Total Number of Pins		544	
		0.0003								
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	2.63	45	88	1.5	45	88		45	88	44
500	2.63	38.1	77.1	1.5	35.9	75.0		35	77	43
450	2.63	31.7	66.9	1.5	27.8	63.0		27	67	41
400	2.63	25.9	57.2	1.5	20.7	52.0		20	57	38
350	2.63	20.7	48.0	1.5	14.6	42.0		14	48	35
300	2.63	16.0	39.4	1.5	9.5	33.0		9	39	31
250	2.63	11.9	31.4	1.5	5.5	25.0		5	31	27
200	2.63	8.4	24.0	1.5	2.4	18.0		2	24	23
	Offset	-8.0		Offset	-14.0					
		Approx. Number of Equations		3536			Total Number of Pins		564	

**Table 4 Number of equations needed for each of the four different Pt Threshold bins as determined by Offset values. Note that this is for only one sign of the tracks.**

Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1000	45	66	10.5	45	66		45	66	22
500	1000	40.9	60.0	10.5	40.2	59.3		40	60	21
450	1000	36.8	54.0	10.5	35.5	52.7		35	54	20
400	1000	32.7	48.0	10.5	31.0	46.3		31	48	18
350	1000	28.6	42.0	10.5	26.6	40.0		26	42	17
300	1000	24.5	36.0	10.5	22.4	33.9		22	36	15
250	1000	20.4	30.0	10.5	18.3	27.9		18	30	13
200	1000	16.3	24.0	10.5	14.4	22.0		14	24	11
Offset	0.0	Offset	-2.0							
	Approx. Number of Equations		715				Total Number of Pins	274		
	0.0003									
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	10.5	45	66	5.2	45	66		45	66	22
500	10.5	40.2	59.3	5.2	39.5	58.6		39	59	21
450	10.5	35.5	52.7	5.2	34.2	51.4		34	53	20
400	10.5	31.0	46.3	5.2	29.3	44.5		29	46	18
350	10.5	26.6	40.0	5.2	24.6	38.0		24	40	17
300	10.5	22.4	33.9	5.2	20.2	31.7		20	34	15
250	10.5	18.3	27.9	5.2	16.1	25.7		16	28	13
200	10.5	14.4	22.0	5.2	12.3	20.0		12	22	11
Offset	-2.0	Offset	-4.0							
	Approx. Number of Equations		729				Total Number of Pins	274		
	0.0003									
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	5.2	45	66	2.63	45	66		45	66	22
500	5.2	39.5	58.6	2.63	38.1	57.1		38	59	22
450	5.2	34.2	51.4	2.63	31.7	48.9		31	51	21
400	5.2	29.3	44.5	2.63	25.9	41.2		25	45	21
350	5.2	24.6	38.0	2.63	20.7	34.0		20	38	19
300	5.2	20.2	31.7	2.63	16.0	27.4		15	32	18
250	5.2	16.1	25.7	2.63	11.9	21.4		11	26	16
200	5.2	12.3	20.0	2.63	8.4	16.0		8	20	13
Offset	-4.0	Offset	-8.0							
	Approx. Number of Equations		1187				Total Number of Pins	304		
	0.0003									
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	2.63	45	66	1.5	45	66		45	66	22
500	2.63	38.1	57.1	1.5	35.9	55.0		35	57	23
450	2.63	31.7	48.9	1.5	27.8	45.0		27	49	23
400	2.63	25.9	41.2	1.5	20.7	36.0		20	41	22
350	2.63	20.7	34.0	1.5	14.6	28.0		14	34	21
300	2.63	16.0	27.4	1.5	9.5	21.0		9	27	19
250	2.63	11.9	21.4	1.5	5.5	15.0		5	21	17
200	2.63	8.4	16.0	1.5	2.4	10.0		2	16	15
Offset	-8.0	Offset	-14.0							
	Approx. Number of Equations		1684				Total Number of Pins	324		

**Table 5 This is the same as table 4 but now for only ½ of the phi range.**

Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1000	45	55	10.5	45	55		45	55	11
500	1000	40.9	50.0	10.5	40.2	49.3		40	50	11
450	1000	36.8	45.0	10.5	35.5	43.7		35	45	11
400	1000	32.7	40.0	10.5	31.0	38.3		31	40	10
350	1000	28.6	35.0	10.5	26.6	33.0		26	35	10
300	1000	24.5	30.0	10.5	22.4	27.9		22	30	9
250	1000	20.4	25.0	10.5	18.3	22.9		18	25	8
200	1000	16.3	20.0	10.5	14.4	18.0		14	20	7
Offset	0.0	Offset	-2.0							
	Approx. Number of Equations		322				Total Number of Pins	154		
	0.0003									
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	10.5	45	55	5.2	45	55		45	55	11
500	10.5	40.2	49.3	5.2	39.5	48.6		39	49	11
450	10.5	35.5	43.7	5.2	34.2	42.4		34	44	11
400	10.5	31.0	38.3	5.2	29.3	36.5		29	38	10
350	10.5	26.6	33.0	5.2	24.6	31.0		24	33	10
300	10.5	22.4	27.9	5.2	20.2	25.7		20	28	9
250	10.5	18.3	22.9	5.2	16.1	20.7		16	23	8
200	10.5	14.4	18.0	5.2	12.3	16.0		12	18	7
Offset	-2.0	Offset	-4.0							
	Approx. Number of Equations		328				Total Number of Pins	154		
	0.0003									
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	5.2	45	55	2.63	45	55		45	55	11
500	5.2	39.5	48.6	2.63	38.1	47.1		38	49	12
450	5.2	34.2	42.4	2.63	31.7	39.9		31	42	12
400	5.2	29.3	36.5	2.63	25.9	33.2		25	37	13
350	5.2	24.6	31.0	2.63	20.7	27.0		20	31	12
300	5.2	20.2	25.7	2.63	16.0	21.4		15	26	12
250	5.2	16.1	20.7	2.63	11.9	16.4		11	21	11
200	5.2	12.3	16.0	2.63	8.4	12.0		8	16	9
Offset	-4.0	Offset	-8.0							
	Approx. Number of Equations		534				Total Number of Pins	184		
	0.0003									
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	2.63	45	55	1.5	45	55		45	55	11
500	2.63	38.1	47.1	1.5	35.9	45.0		35	47	13
450	2.63	31.7	39.9	1.5	27.8	36.0		27	40	14
400	2.63	25.9	33.2	1.5	20.7	28.0		20	33	14
350	2.63	20.7	27.0	1.5	14.6	21.0		14	27	14
300	2.63	16.0	21.4	1.5	9.5	15.0		9	21	13
250	2.63	11.9	16.4	1.5	5.5	10.0		5	16	12
200	2.63	8.4	12.0	1.5	2.4	6.0		2	12	11
Offset	-8.0	Offset	-14.0							
	Approx. Number of Equations		758				Total Number of Pins	204		

**Table 6 This is the same as table 4 but now for only 1/4 of the phi range.**

Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	10.5	45	88	-10.5	45	88		45	88	44
500	10.5	40.2	79.3	-10.5	41.6	80.7		40	81	42
450	10.5	35.5	70.7	-10.5	38.1	73.3		35	73	39
400	10.5	31.0	62.3	-10.5	34.4	65.7		31	66	36
350	10.5	26.6	54.0	-10.5	30.6	58.0		26	58	33
300	10.5	22.4	45.9	-10.5	26.7	50.1		22	50	29
250	10.5	18.3	37.9	-10.5	22.6	42.1		18	42	25
200	10.5	14.4	30.0	-10.5	18.4	34.0		14	34	21
	Offset	-2.0		Offset	2.0					
		Approx. Number of Equations		2520			Total Number of Pins		538	
		0.0003								
Number of sets					1					
Number of LE for equ					2520					
Pt bins					4					
H bins					44.0					
Number of LE for Ser					2969					
Total number of LE					5489		45% of 10K250		82% of 10K130	
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	10.5	45	88	5.2	45	88		45	88	44
500	10.5	40.2	79.3	5.2	39.5	78.6		39	79	41
450	10.5	35.5	70.7	5.2	34.2	69.4		34	71	38
400	10.5	31.0	62.3	5.2	29.3	60.5		29	62	34
350	10.5	26.6	54.0	5.2	24.6	52.0		24	54	31
300	10.5	22.4	45.9	5.2	20.2	43.7		20	46	27
250	10.5	18.3	37.9	5.2	16.1	35.7		16	38	23
200	10.5	14.4	30.0	5.2	12.3	28.0		12	30	19
	Offset	-2.0		Offset	-4.0					
		Approx. Number of Equations		1531			Total Number of Pins		514	
		0.0003								
Number of Sets					2					
Number of LE for equ					3063					
Pt bins					4					
H bins					44.0					
Number of LE for Ser					2969					
Total number of LE					6032		50% of 10K250		91% of 10K130	

**Table 7 The top half of the table is for the Highest Pt Threshold range chip in the 6 chip design, while the bottom is for the High Pt Threshold range.**

Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	5.2	45	88	2.63	45	88		45	88	44
500	5.2	39.5	78.6	2.63	38.1	77.1		38	79	42
450	5.2	34.2	69.4	2.63	31.7	66.9		31	69	39
400	5.2	29.3	60.5	2.63	25.9	57.2		25	61	37
350	5.2	24.6	52.0	2.63	20.7	48.0		20	52	33
300	5.2	20.2	43.7	2.63	16.0	39.4		15	44	30
250	5.2	16.1	35.7	2.63	11.9	31.4		11	36	26
200	5.2	12.3	28.0	2.63	8.4	24.0		8	28	21
	Offset	-4.0	Offset	-8.0						
		Approx. Number of Equations	2493				Total Number of Pins	544		
		0.0003								
Number of sets					1					
Number of LE for equ					2493					
Pt bins					4					
H bins					44.0					
Number of LE for Ser					2969					
Total number of LE					5462		45% of 10K250	82% of 10K130		
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	2.63	45	88	1.75	45	88		45	88	44
500	2.63	38.1	77.1	1.75	36.6	75.7		36	77	42
450	2.63	31.7	66.9	1.75	29.1	64.3		29	67	39
400	2.63	25.9	57.2	1.75	22.4	53.7		22	57	36
350	2.63	20.7	48.0	1.75	16.6	44.0		16	48	33
300	2.63	16.0	39.4	1.75	11.7	35.1		11	39	29
250	2.63	11.9	31.4	1.75	7.6	27.1		7	31	25
200	2.63	8.4	24.0	1.75	4.4	20.0		4	24	21
	Offset	-8.0	Offset	-12.0						
		Approx. Number of Equations	2528				Total Number of Pins	538		
		0.0003								
Number of Sets					1					
Number of LE for equ					2528					
Pt bins					4					
H bins					44.0					
Number of LE for Ser					2969					
Total number of LE					5497		45% of 10K250	83% of 10K130		
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	2.63	45	88	1.5	45	88		45	88	44
500	2.63	38.1	77.1	1.5	35.9	75.0		35	77	43
450	2.63	31.7	66.9	1.5	27.8	63.0		27	67	41
400	2.63	25.9	57.2	1.5	20.7	52.0		20	57	38
350	2.63	20.7	48.0	1.5	14.6	42.0		14	48	35
300	2.63	16.0	39.4	1.5	9.5	33.0		9	39	31
250	2.63	11.9	31.4	1.5	5.5	25.0		5	31	27
200	2.63	8.4	24.0	1.5	2.4	18.0		2	24	23
	Offset	-8.0	Offset	-14.0						
		Approx. Number of Equations	3536				Total Number of Pins	564		
		0.0003								
Number of Sets					1					
Number of LE for equ					3536					
Pt bins					6					
H bins					44.0					
Number of LE for Ser					2969					
Total number of LE					6505		53% of 10K250	98% of 10K130		

**Table 8** This table lists the contents of the next 4 chips in the 6 chip design. The top 1/3 shows the 3<sup>rd</sup> and 4<sup>th</sup> chips that are used for the Medium Pt Threshold. The middle and bottom show the 5<sup>th</sup> and 6<sup>th</sup> chips that are used for the Low. For the middle the minimum Pt is 1.75 GeV, for the bottom it is 1.5.

Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1000	45	88	15	45	88		45	88	44
500	1000	40.9	80.0	15	40.4	79.5		40	80	41
450	1000	36.8	72.0	15	35.9	71.1		35	72	38
400	1000	32.7	64.0	15	31.5	62.8		31	64	34
350	1000	28.6	56.0	15	27.2	54.6		27	56	30
300	1000	24.5	48.0	15	23.0	46.5		23	48	26
250	1000	20.4	40.0	15	19.0	38.5		18	40	23
200	1000	16.3	32.0	15	15.0	30.6		14	32	19
Offset	0.0	Offset	-1.4							
		Approx. Number of Equations	1199				Total Number of Pins	510		
		0.0003								
Number of sets							1			
Number of LE for equ							1199			
Pt bins							1			
H bins							44.0			
Number of LE for Ser							401			
Total number of LE							1600		32% of 10K100	24% of 10K130
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	15	45	88	7.5	45	88		45	88	44
500	15	40.4	79.5	7.5	39.9	79.0		39	80	42
450	15	35.9	71.1	7.5	35.0	70.2		35	71	37
400	15	31.5	62.8	7.5	30.3	61.6		30	63	34
350	15	27.2	54.6	7.5	25.8	53.2		25	55	31
300	15	23.0	46.5	7.5	21.5	45.0		21	47	27
250	15	19.0	38.5	7.5	17.5	37.0		17	39	23
200	15	15.0	30.6	7.5	13.6	29.2		13	31	19
Offset	-1.4	Offset	-2.8							
		Approx. Number of Equations	1210				Total Number of Pins	514		
		0.0003								
Number of Sets							1			
Number of LE for equ							1210			
Pt bins							1			
H bins							44.0			
Number of LE for Ser							407			
Total number of LE							1616		32% of 10K100	24% of 10K130
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	7.5	45	88	5	45	88		45	88	44
500	7.5	39.9	79.0	5	39.4	78.5		39	79	41
450	7.5	35.0	70.2	5	34.1	69.3		34	70	37
400	7.5	30.3	61.6	5	29.1	60.4		29	62	34
350	7.5	25.8	53.2	5	24.4	51.8		24	53	30
300	7.5	21.5	45.0	5	20.0	43.5		20	45	26
250	7.5	17.5	37.0	5	16.0	35.5		15	37	23
200	7.5	13.6	29.2	5	12.2	27.8		12	29	18
Offset	-2.8	Offset	-4.2							
		Approx. Number of Equations	1210				Total Number of Pins	506		
		0.0003								
Number of Sets							1			
Number of LE for equ							1210			
Pt bins							1			
H bins							44.0			
Number of LE for Ser							407			
Total number of LE							1616		32% of 10K100	24% of 10K130
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	5	45	88	3.75	45	88		45	88	44
500	5	39.4	78.5	3.75	38.9	78.0		38	79	42
450	5	34.1	69.3	3.75	33.2	68.4		33	69	37
400	5	29.1	60.4	3.75	27.9	59.2		27	60	34
350	5	24.4	51.8	3.75	23.0	50.4		23	52	30
300	5	20.0	43.5	3.75	18.5	42.0		18	44	27
250	5	16.0	35.5	3.75	14.5	34.0		14	36	23
200	5	12.2	27.8	3.75	10.8	26.4		10	28	19
Offset	-4.2	Offset	-5.6							

**Table 9 This table shows the highest 4 Pt ranges in the 2x8 design.**

Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	3.75	45	88	3	45	88		45	88	44
500	3.75	38.9	78.0	3	38.4	77.5		38	78	41
450	3.75	33.2	68.4	3	32.3	67.5		32	68	37
400	3.75	27.9	59.2	3	26.7	58.0		26	59	34
350	3.75	23.0	50.4	3	21.6	49.0		21	50	30
300	3.75	18.5	42.0	3	17.0	40.5		17	42	26
250	3.75	14.5	34.0	3	13.0	32.5		12	34	23
200	3.75	10.8	26.4	3	9.4	25.0		9	26	18
	Offset	-5.6	Offset	-7.0						
		Approx. Number of Equations		1210			Total Number of Pins	506		
		0.0003								
Number of sets				1						
Number of LE for equ				3629						
Pt bins				1						
H bins				44.0						
Number of LE for Ser				407						
Total number of LE				4036			81% of 10K100	61% of 10K130		
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	3	45	88	2.5	45	88		45	88	44
500	3	38.4	77.5	2.5	37.9	77.0		37	78	42
450	3	32.3	67.5	2.5	31.4	66.6		31	68	38
400	3	26.7	58.0	2.5	25.5	56.8		25	58	34
350	3	21.6	49.0	2.5	20.2	47.6		20	49	30
300	3	17.0	40.5	2.5	15.5	39.0		15	41	27
250	3	13.0	32.5	2.5	11.5	31.0		11	33	23
200	3	9.4	25.0	2.5	8.0	23.6		7	25	19
	Offset	-7.0	Offset	-8.4						
		Approx. Number of Equations		1210			Total Number of Pins	514		
		0.0003								
Number of Sets				1						
Number of LE for equ				3629						
Pt bins				1						
H bins				44.0						
Number of LE for Ser				407						
Total number of LE				4035			81% of 10K100	61% of 10K130		
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	2.5	45	88	2.15	45	88		45	88	44
500	2.5	37.9	77.0	2.15	37.4	76.5		37	77	41
450	2.5	31.4	66.6	2.15	30.5	65.7		30	67	38
400	2.5	25.5	56.8	2.15	24.4	55.6		24	57	34
350	2.5	20.2	47.6	2.15	18.9	46.2		18	48	31
300	2.5	15.5	39.0	2.15	14.1	37.5		14	39	26
250	2.5	11.5	31.0	2.15	10.0	29.5		9	31	23
200	2.5	8.0	23.6	2.15	6.6	22.2		6	24	19
	Offset	-8.4	Offset	-9.8						
		Approx. Number of Equations		1193			Total Number of Pins	512		
		0.0003								
Number of Sets				1						
Number of LE for equ				3580						
Pt bins				1						
H bins				44.0						
Number of LE for Ser				397						
Total number of LE				3977			80% of 10K100	60% of 10K130		
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	2.15	45	88	1.88	45	88		45	88	44
500	2.15	37.4	76.5	1.88	36.9	76.0		36	77	42
450	2.15	30.5	65.7	1.88	29.6	64.8		29	66	38
400	2.15	24.4	55.6	1.88	23.2	54.4		23	56	34
350	2.15	18.9	46.2	1.88	17.5	44.8		17	46	30
300	2.15	14.1	37.5	1.88	12.6	36.0		12	38	27
250	2.15	10.0	29.5	1.88	8.5	28.0		8	30	23
200	2.15	6.6	22.2	1.88	5.2	20.8		5	22	18
	Offset	-9.8	Offset	-11.2						

**Table 10 This table shows the lowest 4 Pt ranges in the 2x8 design.**

Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1000	45	66	5.5	45	66		45	66	22
500	1000	40.9	60.0	5.5	39.5	58.6		39	60	22
450	1000	36.8	54.0	5.5	34.4	51.5		34	54	21
400	1000	32.7	48.0	5.5	29.5	44.7		29	48	20
350	1000	28.6	42.0	5.5	24.8	38.2		24	42	19
300	1000	24.5	36.0	5.5	20.5	31.9		20	36	17
250	1000	20.4	30.0	5.5	16.4	25.9		16	30	15
200	1000	16.3	24.0	5.5	12.5	20.2		12	24	13
Offset	0.0	Offset	-3.8							
		Approx. Number of Equations	1151				Total Number of Pins	298		
		0.0003								
Number of sets				1						
Number of LE for equ				1151						
Pt bins				4						
H bins				22.0						
Number of LE for Ser				1590						
Total number of LE				2741			55% of 10K100	41% of 10K130		
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	5.5	45	66	2.75	45	66		45	66	22
500	5.5	39.5	58.6	2.75	38.2	57.3		38	59	22
450	5.5	34.4	51.5	2.75	31.9	49.1		31	52	22
400	5.5	29.5	44.7	2.75	26.2	41.5		26	45	20
350	5.5	24.8	38.2	2.75	21.0	34.4		21	38	18
300	5.5	20.5	31.9	2.75	16.4	27.8		16	32	17
250	5.5	16.4	25.9	2.75	12.3	21.8		12	26	15
200	5.5	12.5	20.2	2.75	8.7	16.4		8	20	13
Offset	-3.8	Offset	-7.6							
		Approx. Number of Equations	1156				Total Number of Pins	298		
		0.0003								
Number of Sets				1						
Number of LE for equ				1156						
Pt bins				4						
H bins				22.0						
Number of LE for Ser				1590						
Total number of LE				2746			55% of 10K100	41% of 10K130		
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	2.75	45	66	1.84	45	66		45	66	22
500	2.75	38.2	57.3	1.84	36.8	55.9		36	57	22
450	2.75	31.9	49.1	1.84	29.5	46.7		29	49	21
400	2.75	26.2	41.5	1.84	22.9	38.2		22	41	20
350	2.75	21.0	34.4	1.84	17.2	30.6		17	34	18
300	2.75	16.4	27.8	1.84	12.3	23.8		12	28	17
250	2.75	12.3	21.8	1.84	8.2	17.8		8	22	15
200	2.75	8.7	16.4	1.84	5.0	12.6		4	16	13
Offset	-7.6	Offset	-11.4							
		Approx. Number of Equations	1146				Total Number of Pins	296		
		0.0003								
Number of Sets				1						
Number of LE for equ				1146						
Pt bins				4						
H bins				22.0						
Number of LE for Ser				1590						
Total number of LE				2736			55% of 10K100	41% of 10K130		
Layer	Max Pt	LH Edge	RH Edge	Min Pt	LH Edge	RH Edge		Min	max	Diff
550	1.84	45	66	1.38	45	66		45	66	22
500	1.84	36.8	55.9	1.38	35.5	54.6		35	56	22
450	1.84	29.5	46.7	1.38	27.0	44.2		27	47	21
400	1.84	22.9	38.2	1.38	19.7	35.0		19	38	20
350	1.84	17.2	30.6	1.38	13.4	26.8		13	31	19
300	1.84	12.3	23.8	1.38	8.2	19.7		8	24	17
250	1.84	8.2	17.8	1.38	4.2	13.7		4	18	15
200	1.84	5.0	12.6	1.38	1.1	8.8		1	13	13
Offset	-11.4	Offset	-15.2							

**Table 11** This table shows all the chips in the 2x2x4 design.